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Deliver to: Examiner Luan Thai
Firm Name: USPTO
Fax Number: (703) 746-3906 **Telephone No.:** (703) 308-1211
From: Libby Hope
Date: August 20, 2002 **Time:** 1:25 P.M. MDT
Matter: Application Serial No. 09/741,535 (Our Docket No.: 42390P9482)
Number of pages including cover sheet: 6

Examiner Thai:

The purpose of my request for an Examiner interview at this stage is to see if we can come to an agreement on a set of allowable claims. I am proposing the attached claimset, and arguments as to why my client does not believe these claims are anticipated or made obvious by the prior art of record. Also, any suggestions you have would be greatly appreciated.

If you need anything else, please do not hesitate to contact me, or my secretary, Debbie Peloquin at the number shown above.

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PROPOSED CLAIMS

Application Serial No. 09/741,535

1. (Twice Amended) A method comprising:

placing an incomplete chip package into a mold formed by a first portion and a second portion, the incomplete chip package comprising a chip and a substrate electrically coupled using a flip chip process, the mold having an upper inner surface in which its entire length is coated with release film, and the chip having (i) a top surface facing the substrate, (ii) a bottom surface opposite the top surface, the bottom surface butting against the upper inner surface, and (iii) one or more side surfaces between the top and bottom surfaces;

injecting a liquid resin into a runner section of the mold, the runner formed [betweem] between a first portion and the second portion, and the resin encapsulating a significant portion of the one or more side surfaces, and filling a first gap between the top surface and the adjacent substrate; and

curing the resin.

20. (Twice Amended) A method comprising:

placing an incomplete flip chip package into a bottom inner cavity of a bottom mold portion[;], the incomplete flip chip package

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comprising a chip and a substrate, the chip having a top surface coupled by reflowed solder bumps to [a] an upper surface of the substrate, the chip further comprising a bottom surface opposite the top surface and one or more side surfaces between the top and bottom surfaces;

mating an upper mold portion with the lower mold portion, the upper mold portion having an upper inner cavity, including an upper inner surface in which its entire length is coated with a release film, and the bottom surface of the chip butts against the upper inner surface, the upper and bottom inner cavities forming a mold inner cavity enclosing the incomplete flip chip package, and forming a runner between the upper and lower mold portions;

injecting a predetermined amount of a liquid resin into the mold inner cavity through the runner, the liquid resin encapsulating substantially all or the one or more side surfaces and substantially all of the upper surface, the liquid resin further filling a gap between the top surface of the chip and an adjacent portion of the upper surface of the substrate, encapsulating the reflowed solder bumps; and

curing the liquid resin by maintaining the mold at an elevated temperature for a predetermined period of time, the elevated temperature being

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equal to or greater than the cure temperature of the filled liquid resin for the predetermined period of time.

33. (New) The method of claim 1, additionally comprising separating the mold between the upper mold portion and the lower mold portion to expose a molded chip package, the upper mold portion being removed with the release film.

34. (New) The method of claim 20, additionally comprising separating the mold between the upper mold portion and the lower mold portion to expose a molded chip package, the upper mold portion being removed with the release film.

35. (New) A molded flip chip package comprising solidified resin formed by:

placing an incomplete chip package into a mold formed by a first portion and a second portion, the incomplete chip package comprising a chip and a substrate electrically coupled using a flip chip process, the mold having an upper inner surface in which its entire length is coated with release film, and the chip having (i) a top surface facing the substrate, (ii) a bottom surface opposite the top surface, the bottom surface butting against the upper inner surface, and (iii) one or more side surfaces between the top and bottom surfaces;

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injecting a liquid resin into a runner section of the mold, the runner formed between a first portion and the second portion, and the resin encapsulating a significant portion of the one or more side surfaces, and filling a first gap between the top surface and the adjacent substrate; and

curing the resin.

36. (New) The method of claim 35, additionally comprising separating the mold between the upper mold portion and the lower mold portion to expose a molded chip package, the upper mold portion being removed with the release film.

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Lin does not teach or disclose the following:

1. release film that is coated along entire length of the upper inner cavity: in Lin, a tape is placed in the mold cavity such that it makes contact with the backside of the die (see reference numeral 38 in FIGS. 3 and 4), but not with the entire length of the top mold platen.
2. an upper inner surface that is coated with release film: in Lin, the tape is such that it adheres better to silicon than to the top mold platen, so that the tape adheres to the inactive backside of the die when the molded unit is ejected from the mold cavity.
3. release film that is removed with the upper mold portion: see item #2.

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